Low Phase Noise Frequency Synthesiser for the Trapped Atom Clock on a Chip

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***Abstract*—We report on the realisation of a $6.834\,\mathrm{GHz}$ synthesis chain for the Trapped Atom Clock on a Chip (TACC) that is being developed at LNE-SYRTE. The stability of the chain is 10^{-14} at $1\,\mathrm{s}$, one order of magnitude below the stability goal of TACC. This ensures that the synthesizer will not be a limiting factor of the clock performance. The chain is based on the frequency multiplication of a $100\,\mathrm{MHz}$ reference signal to $6.4\,\mathrm{GHz}$. It uses a comb generator based on a monolithic GaAs non-linear transmission line. This is a novelty in the fabrication of high stability microwave synthesisers.**

I. Introduction

The stability of an atomic clock improves with the time during which the atomic resonance can be probed. This is above all limited by the time during which the atomic motion is controlled. The implementation of laser cooling techniques reduces the mean atomic velocity to a few $\mathrm{cm/s}$, giving access to observation times of hundreds of milliseconds. Examples are the atomic fountain clocks, in which gravity is compensated by launching the atoms on a vertical parabola [2]. Alternatively, gravity and the residual thermal expansion can be counteracted by keeping the atoms in a trap [3]. Microwave interrogation of trapped atoms combines long observation times with the spectral purity of well-managed electronics. Here we present the construction and evaluation of a low phase noise microwave synthesiser for the interrogation of the trapped atom clock currently under construction in our laboratory [4].

Our trapped atom clock is based on a two photon transition between the hyperfine states of the ^{87}Rb ground state, one photon being in the microwave domain ($\sim 6.834\,\mathrm{GHz}$), the second in the radio-frequency domain ($\sim 2\,\mathrm{MHz}$). A Ramsey, two pulse method is used for interrogating a sample of ultra-cold atoms ($\sim 300\,\mathrm{nK}$) collected in a magnetic trap generated by an atom chip. The magnetic trapping relies on the interaction between the atomic magnetic moment depending on the atomic quantum numbers and a position dependant magnetic field. Therefore, the clock states have been chosen as $|1\rangle \equiv |F=1, m_F=-1\rangle$ and $|2\rangle \equiv |F=2, m_F=1\rangle$, which are both low magnetic field seekers and can be trapped. The use of the atom chip technology [5] enables the realisation of a compact litre-size apparatus.

The principle of the atom chip clock was demonstrated by Treutlein *et al.* [5]. They measured the frequency stability relative to a reference quartz oscillator (Oscilloquartz OCXO 8607-BM). The Allan standard deviation of the fractional-frequency fluctuation of their set-up was found to decrease as $\sigma_y(\tau) = 1.7\times10^{-11}\mathrm{s}^{1/2}\tau^{-1/2}$ for $\tau < 6\times10^2\,\mathrm{s}$. The long-term drift of the interrogation oscillator led to a departure from the $\tau^{-1/2}$ tendency above $6\times10^2\,\mathrm{s}$. Simple technical improvements to the atom chip clock identified by the authors of [5], such as magnetic shielding and shot-noise limited detection should decrease the stability to $\sim 10^{-12}\mathrm{s}^{1/2}\tau^{-1/2}$. More advanced improvements including increase of the number of atoms and reduction of dead times have been shown to enable a clock stability in the low $10^{-13}\mathrm{s}^{1/2}\tau^{-1/2}$ range [6].

In this work we describe the construction and evaluation of a low phase noise synthesizer for the $6.834\,\mathrm{GHz}$ microwave component of the clock interrogation. Full computer control is garantied for frequency tuning and output power. Phase noise measurements between two identical systems confirm no significant degradation of the $100\,\mathrm{MHz}$ local reference oscillator. Referencing to a high stability quartz or the SYRTE's internal distribution signal should guarantee a frequency stability below $10^{-13}\mathrm{s}^{1/2}\tau^{-1/2}$ such as not to degrade the clock stability.

II. Synthesiser layout and methods

The synthesiser's purpose is to generate the $6.834\,\mathrm{GHz}$ clock interrogation signal by multiplication from a $100\,\mathrm{MHz}$ reference signal (fig. 1). The reference signal is provided by a quartz included in the synthesiser which may operate as stand-alone or may be locked to the SYRTE's reference signal distributed from a cryogenic sapphire oscillator having a relative frequency stability of the order of 10^{-15} between 1 and $1000\,\mathrm{s}$ [7]. The quartz' output, also assuring constant power is distributed among the different arms of the synthesiser. The multiplication arm is shown in the centre of figure 1, where a non-linear transmission line (NLTL) generates a $6.4\,\mathrm{GHz}$ signal. It phase-stabilises a dielectric resonator oscillator (DRO) where the $34\,\mathrm{MHz}$ beat signal is compared to a direct digital synthesiser (DDS) allowing frequency tuning. A separate arm generates a $400\,\mathrm{MHz}$ signal controllable in power, which is mixed to the DRO output to constitute the interrogation signal.

To assure the synthesiser's performance we built two identical systems and carry out homodyne phase measurements.

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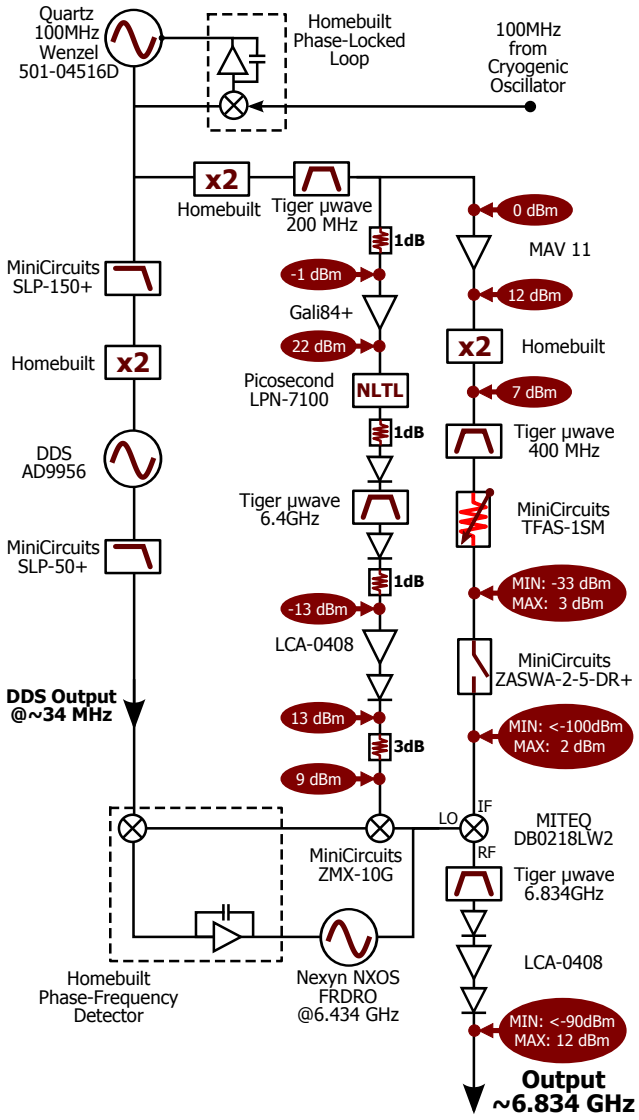

Fig. 1. Schematic of our synthesiser generating the 6.834 GHz atomic clock interrogation signal. A 100 MHz quartz oscillator supplies the synthesiser's reference, which may be lock to the SYRTE's reference signal distributed from a cryogenic sapphire oscillator. In the centre of the image, a non-linear transmission line creates a stable 6.4 GHz signal, which in combination with a DDS locks a dielectric resonator oscillator. A further 400 MHz signal is added to the DRO output allowing easy power control.

Both systems are fed with the same reference signal and their outputs are added in quadrature in a phase detector. The DC output is low-pass-filtered (< 195 kHz), amplified and analysed by means of a FFT spectrum analyser. Measurements are taken after each crucial step in the generation process. They are described in detail in the following.

III. The Reference

The synthesiser's reference is a 100 MHz quartz oscillator (Wenzel Associates, Inc. Standard 100 MHz-SC Sprinter Crystal Oscillator, P/N 501-04516) which may be locked to an external reference via a phase looked loop (PLL). In order to take advantage of quartz' characteristics, the PLL bandwidth is chosen to be approximately 100 Hz. This way, the quartz's drift below 100 Hz is compensated by the lock, while at high frequencies it is running freely. The NLTL-based synthesisers described by Boudot *et al.* [8] utilise a similar method for transferring the stability of an external oscillator of superior quality to the synthesiser local reference. The synthesiser's frequency stability reported in [8] is 10^{-14} at 1 s, which is consistent with the stability of the system reported in the present work.

IV. Frequency Multiplication

To up-convert the 100 MHz reference signal into the microwave regime we use a monolithic GaAs non-linear transmission line (NLTL) (Picosecond Pulse Labs, Model 7100). Such comb generators present several advantages with respect to other methods of frequency multiplication: low phase noise, wide range of input frequencies, low input power, and high output power at high harmonics [8], [9]. The reference signal is frequency doubled to 200 MHz in a homebuilt device and band pass filtered before being split into the multiplication arm and the RF arm. The use of a higher input frequency to the NLTL increases the power in each harmonic as well as the harmonic spacing, which in turn simplify harmonic selection and filtering. The 32th harmonic is selected and amplified to provide 9 dBm at 6.4 GHz.

We measure the phase noise of the frequency doubler, the 200 MHz amplifier (Mini-Circuits Gali84+) and the 6.4 GHz micro-wave signal. Two identical systems are built, both referenced to the same quartz. The phase noise is measured using a PD-121 phase detector at 200 MHz. The base noise of this measuring system has a white noise floor of -160 dBrad^2/Hz, while the flicker phase component is $<$ -140 dBrad^2/Hz at 1 Hz. The noise introduced by the homebuilt doubler is comparable to the detection limit excluding a degradation of the reference signal.

Amplification of the 200 MHz signal provides the necessary power of 20 to 24 dBm to the NLTL's input. This amplification is probably the most sensitive section of the synthesiser. In the linear operation regime, the chosen amplifiers gain is slightly more than 23 dB. The 1 dB compression point occurs at an input value of -1 dB, where the amplifier output is approximately 22 dBm. We found that when operated at the 1 dB compression point the amplifier's phase noise is characterised by a phase flicker component of -115 dBrad^2/Hz at 1 Hz. An example of our measurements, scaled to 6.4 GHz, is shown in figure 2. This performance fulfils the stability requirement.

To evaluate the 6.4 GHz signal output from the NLTL after it is amplified (Miteq LCA-0408), a double balanced mixer (MiniCircuits, ZMX10-G+) is used. Its output is low pass filtered ($f_c = 195$ kHz) and amplified giving a sensitivity limited by a flicker phase noise component below -120 dBrad^2/Hz at 1 Hz and a white noise floor of -150 dBrad^2/Hz. Figure 2 compares the NLTL's phase noise curves measured for two input powers of 20 dBm (green) and 22 dBm (blue). We measure a flicker phase noise of -85 dBrad^2/Hz at 1 Hz

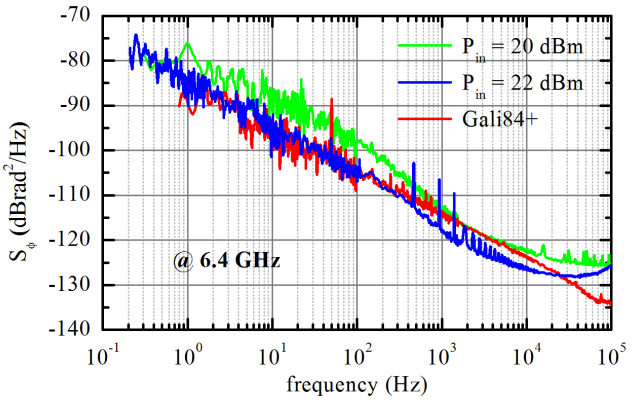

Fig. 2. Phase noise of the non linear transmission line for different input powers. A Gali84+ amplifier feeds 200 MHz into the NLTL which generates a comb of harmonics. The phase measurement is performed at 6.4 GHz between two identical systems. For comparison the phase noise measured at the amplifier output scaled to 6.4 GHz is shown. When operated near the 1 dB compression point, the Gali84+ output (red curve) is dominated by flicker phase noise of -85 dBrad^2/Hz at a 1 Hz offset frequency. The best multiplication result is obtained when driving the NLTL at 22 dBm, which corresponds to the amplifier's 1 dB compression point. Here the NLTL does not degrade the amplifier noise. In contrast, only 2 dBm less of input power are sufficient for a considerable increase at all Fourier frequencies.

offset frequency. The curves are compared to the 200 MHz measurement at the output of the Gali84+ amplifiers when operated at the 1 dB compression point scaled to 6.4 GHz (red). The comparison shows no degradation by the multiplication for the 22 dBm input. Therefore, the amplifier's 1 dB compression point has been identified as the optimum operation.

This phase noise measurement can be summarised by

$$S_\phi(f) = b_{-1} f^{-1} \tag{1}$$

with $b_{-1} = 10^{-8.5}$. In this case, the phase noise power spectral density is converted in the Allan variance of the fractional frequency fluctuations utilising the expression provided by E. Rubiola in [10]

$$\sigma_y(\tau) = [1.038 + 3\ln(2\pi f_H \tau)] \times \frac{h_1}{(2\pi)^2}\tau^{-2} \tag{2}$$

where $h_1 = b_1/\nu_0^2$, ν_0 is the carrier frequency and f_H is the low-pass cutoff frequency. Combining $b_{-1} = 10^{-8.5}$ with $\nu_0 = 6.4$ GHz and $f_H = 195$ kHz, a frequency stability of $\sim 9\times10^{-15}$ at 1 s is calculated. This is one order of magnitude below the projected clock stability.

V. Dielectric Resonator Oscillator

The synthesiser's principal microwave signal, at 6.434 GHz, is provided by a dielectric resonator oscillator (Nexyn NXOS-EFC-0643-02140). Frequency tuning is possible mechanically within $\pm$15 MHz and electrically within 6 MHz. Electric locking to the 6.4 GHz signal and a 34 MHz DDS signal assures its phase stability. In this pursuit the DRO output is mixed with the 6.4 GHz signal to produce a beat note near 34 MHz which in turn is compared to a DDS via a homebuilt phase-frequency detector. The detector produces an error signal that is fed back into the DRO. Thereby the DDS (see section VI) defines the DRO's frequency and allows tuning.

To test the DRO, the 100 MHz output of a free running quartz has been split and fed to two identical systems, each consisting of a 6.4 GHz multiplication chain and a DRO. The DROs are stabilised by means of two phase frequency detectors. A single DDS, clocked by the quartz signal, is used to provide the tuning signal. The two DRO signals are compared in quadrature in the doubled balanced mixer. The result, scaled to 6.834 GHz, is included in figure 4. The graph also repeats the phase noise of the NLTL already shown in fig 2, now scaled to 6.834 GHz. Comparing the two, it becomes obvious that the phase flicker signature of the NLTL has been preserved by the locked DRO. For Fourier frequencies of the order 1 kHz, the DRO measurement shows the influence of the phase-frequency detector, giving a 10 dB noise increase near the lock bandwidth.

VI. Frequency tuning via DDS

The DRO frequency is fine tuned via the 34 MHz offset signal generated from a direct digital synthesiser (Analog Devices, AD9956 on evaluation board Z, Rev. E). The DDS is computer controlled via ethernet or serial communication by means of an Acme Systems FOX Board LX832. The digital to analog conversion generates, besides the desired frequency f_{DDS} an image frequency at $f_{Clock} - f_{DDS}$. Therefore, we choose the maximum possible clock frequency. A separate arm, split from the quartz's 100 MHz signal (figure 1) is frequency doubled and input to the DDS. In addition, a 50 MHz low pass filter cleans the DDS output.

VII. Power control and signal switching

The clock interrogation signal is finally obtained by adding a fixed frequency 400 MHz signal to the DRO output. This signal originates from a third arm derived from the quartz, is frequency doubled twice and mixed in a doubled balanced mixer (MITEQ DB0218LW2) (figure 1). The purpose of this separate RF-signal is to enable a DRO frequency well below the atomic resonance, such that any microwave leakage will not disturb the clock transition. Secondly, controlling the RF power provides an easy way to control the final output power, including fast switching. A TTL controlled switch (Mini-Circuits ZASWA-2-5-DR+) is used to switch-on and off the clock interrogation signal in less that 5 µs with 60 dB attenuation. The on-power is set by means of a voltage controlled attenuator (Mini-Circuits TFAS-1SM) where a 25 dB variation at 6.834 GHz is obtained for a control voltage of 0.5 ± 0.2 V (figure 3). Switch and attenuator together provide a maximum attenuation of 100 dB measured at the synthesiser's $\sim$ 6.834 GHz output.

To investigate the phase shift introduced by the switch and the attenuator, we experimentally simulate the pulsed operation of the clock interrogation. A 5 kHz square wave modulation alternating between 0 and 5 V is supplied simultaneously to

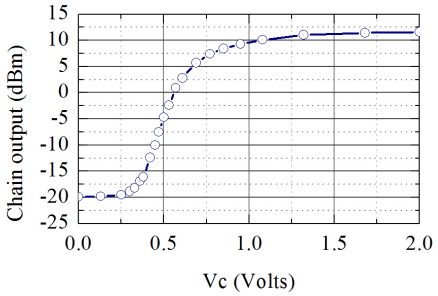

Fig. 3. The output power at 6.834 GHz as a function of the control voltage applied to the 400 MHz attenuator. A 25 dB variation is obtained for a control voltage of 0.5 ± 0.2 V. When the attenuator is combined with a TTL controlled switch, a maximum attenuation of 100 dB is achieved.

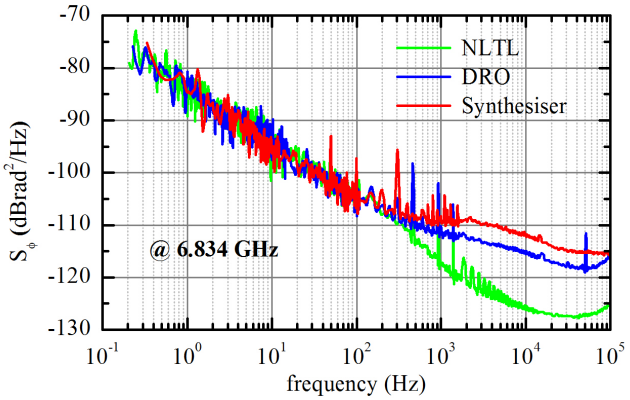

Fig. 4. Phase noise of the complete synthesiser (red) measured in comparing two systems build by independent groups. For comparison the phase noise of the non linear transmission line (green) and the locked dielectric resonator oscillator (blue) are given scaled to 6.834 GHz. It is obvious that the determining element is the NLTL and the amplification stage utilised for its input.

the control ports of both the switch and the attenuator. Both devices are then put together into one arm of a 400 MHz interferometric system. A phase detector based on a Mini-Circuits TUF-3+ frequency mixer detects the temporal variation of the phase induced by the switch and attenuator combination. The measurements show that the relative phase is stabilised in less than 5 µs. This time includes a 2 µs lag between the rising edge of the control modulation (switch-on) and the rising edge of the phase detector signal, and a ~ 1.5 µs $1/e$ time constant for the relative phase to stabilise to a constant value.

VIII. Synthesiser output

The stability of the complete synthesiser is tested by comparing it to the output of a second very similar system. The second synthesiser, which also relies on a NLTL for frequency multiplication, has been built by an independent group of the same laboratory. Starting from the same 100 MHz reference signal, both synthesisers are tuned to 6.834 GHz using separate DDSs. The two microwave signals are fed in quadrature into a doubled balance mixer (MITEQ DB0218LW2), the output of which is low-pass-filtered and amplified. The result of this measurement is shown in red in figure 4. This measurement shows that for Fourier frequencies below ~ 1 kHz, the purity of the signal generated by the multiplication arm of these synthesisers is successfully transferred to the output signal. Above the 1 kHz offset frequency, the bandwidth of the DRO phase-frequency detector is observed as an increase of the phase noise curve. This is indeed confirmed by varying the gain of the phase-frequency lock of the second synthesiser, which results in a variation of the difference between the blue and the red curves shown in figure 4. The results shown in figure 4 demonstrate that the a frequency stability of $\sim 9 \times 10^{-15}$ at 1 s is maintained by the synthesiser output.

IX. Conclusion

A low noise microwave synthesiser has been realised for the trapped atom clock on a chip. The stability goal of this atomic clock is estimated to be of the order of 10^{-13} at 1 s. Proper characterisation and careful optimisation of the synthesiser constituents results in a low flicker phase noise of -85 dBrad^2/Hz at an 1 Hz offset frequency. This corresponds to a frequency stability below 10^{-14} at 1 s, one order of magnitude better that the level estimated for the clock.

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